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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,176	12/04/2003	Rose Mulligan	42P16008	8588
8791	7590	03/22/2006	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN			CHEN, JACK S J	
12400 WILSHIRE BOULEVARD			ART UNIT	
SEVENTH FLOOR			PAPER NUMBER	
LOS ANGELES, CA 90025-1030			2813	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

A

Office Action Summary	Application No.	Applicant(s)	
	10/729,176	MULLIGAN, ROSE	
	Examiner	Art Unit	
	Jack Chen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 December 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 4-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,2,4-7 and 13 is/are allowed.
- 6) ☒ Claim(s) 8-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication 2004/0232524 A1 (**Howard et al.**).

Howard discloses, a process comprising: dicing a semiconductor wafer before forming devices on the semiconductor wafer (paragraph 0051), the dicing/scribing forming trenches 107 in the semiconductor wafer 100 by etching (paragraph 0017); forming an oxide in the trenches formed by dicing the semiconductor (paragraph 0025); forming the semiconductor devices on the diced semiconductor wafer (paragraph 0026); removing the oxide from the trenches after the devices are formed (paragraph 0027); back-grinding the semiconductor wafer after forming the devices on the semiconductor wafer (paragraphs 0052 and 0056).

The prior art **Howard**, as explained above, discloses each of the claimed features except for indicating the depth of the trenches is 90 to 150 microns from the surface of the semiconductor wafer. **Howard** does however teach,

“[0018] Depth 105a and width 107 of the trench are correlated by the aspect ratio depth-to-width, which is achievable by the selected etching technique. For plasma etching technology, the aspect ratio is preferably 8:1 or less (such as 6:1 or 4:1). As an example, a trench depth of 20 μm would require a trench width of approximately 2 to 3 μm . For shallower trenches, a trench width of about 1 μm or even 0.5 μm is achievable.”

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And regarding the embodiments wherein backside grinding is used to form the trenches 107, **Howard** states in paragraph (0046),

“in this embodiment, the trench streets may have to be etched deeper than in the previously described embodiments, since the trench streets have to penetrate the whole depth of the intended final wafer thickness”

Accordingly, the depth of the trench can be optimized depending upon the method of forming the trenches. In this regard, it has been held that

“Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed ‘critical ranges’ and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” *In re Aller* 105 USPQ233, 255 (CCPA 1955).

See also In re Waite 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmscher* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

According to precedent, then, and the teachings of **Howard**, the choice of trench depth is a matter of routine optimization, and one of ordinary skill would be motivated to use the depth of

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90 to 150 microns in order to form a trench of optimum depth and to avoid the saw from coming too close to the electronic devices formed in the semiconductor wafer.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Howard** as applied to claims 8-10 above, and further in view of US 5,414,297 (**Morita et al.**).

The prior art of **Howard**, as explained above, discloses each of the claimed features except for indicating that the oxide filling the trench is planarized.

Morita teach forming and planarizing an insulating film 46 in "along the entirety of the scribe line 2" before forming the semiconductor devices and singulating the wafer in to dice (fig. 2a-2e; Title; Abstract; col. 9, lines 20-54).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to make the oxide fill of **Howard** planar, in order to correct any unevenness in height prior to formation of the semiconductor devices, as taught by **Morita**. A planar topography aids alignment of the wafer for subsequently deposited device layers.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Howard** in view of **Morita** as applied to claim 8-11 above, and further in view of US 5,716,495 (**Butterbaugh et al.**).

The prior art of **Howard** in view of **Morita**, as explained above, discloses each of the claimed features except that Howard does not indicate how the oxide in the trench is removed.

Butterbaugh teaches the benefits of using a UV laser to remove oxide and contaminants from a semiconductor wafer with good control of the endpoint.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use a UV laser to remove the oxide of Howard, because Howard is silent to the method of

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removing the oxide such that one of ordinary skill would be motivated to use known methods that have additional benefits such as removing contaminants, such as that taught in Butterbaugh.

Reasons For Allowance

Claims 1-2, 4-7 and 13 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance: claims 1-2, 4-7 and 13 are allowed for reasons deemed to be of record.

NOTE: the limitation of claim 3, such as "further comprising scribing the trenches" is allowable in combination with other claimed limitations as recited in claim 1.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

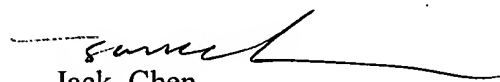
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however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent - Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Jack Chen
Primary Examiner
Art Unit 2813

March 20, 2006